**GOVT POLYTECHNIC MANESAR**

**LESSON PLAN**

Faculty’s Name : Mrs. Reena Devi

Department : Computer Engineering

Semester : Third

Subject : Digital Electronics

Duration : 15 Weeks (July, 2018 - Nov,2018)

**\*\*** **Work Load (Lecture/Practical) per Week in Hours Lectures-04, Practical-04**

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| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  | **Theory** |  |  | **Practical** |
| **Week** |  |  |  |  |  |  |
|  |  | **Topic** |  | **(Including** |  | **Topic** |
|  | **day** |  |  | **assignment / test)** | **Day** |
|  |  |  |  |
| 1st |  |  | **1. Introduction** |  |  | Verification and interpretation of truth |
|  | 1st |  | a) Distinction between analog and digital signal. | 1st | tables for AND, OR, NOT gates |
|  |  |  |  |  |  |
|  |  |  | b) Applications and advantages of digital signals. |  | Verification and interpretation of truth |
|  | 2nd |  |  |  |  | 2nd | tables for AND, OR, NOT gates |
|  |  |  |  |  |  |  |
|  |  |  | **2. Number System** |  |  | Verification and interpretation of truth |
|  | 3rd |  | a) Binary, octal and hexadecimal number system: | 3rd | tables for AND, OR, NOT gates |
|  |  | Conversion from decimal to binary |  |
|  |  |  |  |  |  |
| 2nd | 1st |  | Conversion from hexadecimal to binary | 1st | Verification and interpretation of truth |
|  |  |  |  |  | tables for NAND, NOR gates |
|  |  |  |  |  |  |
|  | 2nd |  | Conversion from binary to decimal | 2nd | Verification and interpretation of truth |
|  |  |  |  |  | tables for NAND, NOR gates |
|  |  |  |  |  |  |
|  |  |  | Conversion from binary to hexadecimal |  | Verification and interpretation of truth |
|  | 3rd |  |  |  |  | 3rd | tables for Exclusive OR (EXOR) gate |
|  |  |  |  |  |  |
| 3rd |  |  | b) Binary addition and subtraction including |  | Verification and interpretation of truth |
|  | 1st |  | binary points. 1’s and 2’s | complement method | 1st | tables for Exclusive OR (EXOR) gate |
|  |  |  | of addition/subtraction. |  |  |  |
|  |  |  | **3. Codes and Parity** |  |  | Verification and interpretation of truth |
|  | 2nd |  | a) Concept of code, weighted and non-weighted | 2nd | tables for Exclusive OR (EXOR) gate |
|  |  |  | codes |  |  |  |  |
|  |  |  | Examples of 8421, BCD,Excess-3 and Gray |  | Verification and interpretation of truth |
|  | 3rd |  | code. |  |  | 3rd | tables forExclusive NOR(EXNOR) gate |
|  |  |  |  |  |  |
| 4th |  |  | b) Concept of parity, single and double parity, |  | Verification and interpretation of truth |
|  | 1st |  | Error detection |  |  | 1st | tables forExclusive NOR(EXNOR) gate |
|  |  |  |  |  |  |
|  |  |  | **4. Logic Gates and Families** |  | Verification and interpretation of truth |
|  | 2nd |  | a) Concept of negative and positive logic | 2nd | tables forExclusive NOR(EXNOR) gate |
|  |  |  | b) Definition, symbols and truth tables of NOT, |  |  |
|  |  |  |  |  |  |
|  |  |  | NAND & NOR as universal gates. |  | Realisation of logic functions with the |
|  | 3rd |  | (c) Introduction to TTL and CMOS logic | 3rd | help of NAND gate |
|  |  |  | families |  |  |  |  |
| 5th |  |  | **5. Logic Simplification** |  |  | Realisation of logic functions with the |
|  | 1st |  | a) Postulates of Boolean algebra, De Morgan’s | 1st | help of NAND gate |
|  |  |  | Theorems. |  |  |  |  |

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| --- | --- | --- | --- | --- |
|  | 2nd | Implementation of Boolean (logic) equation with | 2nd | Realisation of logic functions with the |
|  | gates |  | help of NOR gate |  |
|  |  |  |  |  |
|  | 3rd | Implementation of Boolean (logic) equation with | 3rd | Realisation of logic functions with the |
|  | gates |  | help of NOR gate |  |
|  |  |  |  |  |
| 6th |  | Karnaugh map (2 variables) and simple |  | To design a half adder using XOR gate |
|  | 1st | application in developing combinational logic | 1st | and verification of its | operation |
|  |  | circuits |  |  |  |  |
|  |  |  |  |  |
|  |  | Karnaugh map (3 variables) and simple |  | To design a half adder using XOR gate |
|  | 2nd | application in developing combinational logic | 2nd | and verification of its | operation |
|  |  | circuits |  |  |  |  |
|  |  |  |  |  |
|  |  | Karnaugh map (4 variables) and simple |  | To design a half adder using NAND |
|  | 3rd | application in developing combinational logic | 3rd | gate and verification of its |
|  |  | circuits |  |  | operation |  |
|  |  |  |  |  |
| 7th |  | Karnaugh map (4 variables) and simple |  | To design a half adder using NAND |
|  | 1st | application in developing combinational logic | 1st | gate and verification of its |
|  |  | circuits |  |  | operation |  |
|  |  |  |  |  |  |
|  |  | **6. Arithmetic circuits** |  |  | Construction of a full adder circuit |
|  | 2nd | Half adder circuit, design and implementation. | 2nd | using XOR gate and verify its |
|  |  |  |  |  | operation |  |
|  |  |  |  |  |  |
|  |  |  |  |  | Construction of a full adder circuit |
|  | 3rd | Full adder circuit, design and implementation. | 3rd | using NAND gate and verify its |
|  |  |  |  |  | operation |  |
| 8th |  | 4 bit adder circuit |  |  | Construction of a full adder circuit |
|  | 1st |  |  | 1st | using NAND gate and verify its |
|  |  |  |  |  | operation |  |
|  |  |  |  |  |
|  |  | **7. Decoders, Multiplexeres, De Multiplexeres** |  | Verification of truth table for positive |
|  |  | **and Encoder** |  |  | edge triggered IC flip-flops of D latch |
|  | 2nd | a) Four bit decoder circuits for 7 segment display | 2nd |  |  |
|  |  | and decoder/driver ICs. |  |  |  |  |
|  |  |  |  |  |
|  | 3rd | b) Basic functions and block diagram of MUX | 3rd | Verification of truth table for positive |
|  | with different Ics |  | edge triggered IC of D flip-flop |
|  |  |  |  |  |
| 9th | 1st | b) Basic functions and block diagram of | 1st | Verification of truth table for positive |
|  | DEMUX with different Ics |  | edge triggered IC of JK flip-flops. |
|  |  |  |  |  |
|  |  | c) Basic functions and block diagram of |  | Verification of truth table for Negative |
|  | 2nd | Encoder |  | 2nd | edge triggered IC flip-flops of D latch |
|  |  |  |  |  |  |
|  |  | **8. Latches and flip flops** |  |  | Verification of truth table for negative |
|  | 3rd | a) Concept and types of latch with their working | 3rd | edge triggered IC of D flip-flop |
|  |  | and applications |  |  |  |  |
|  |  |  |  |  |
| 10th | 1st | b) Operation using waveforms and truth tables of | 1st | Verification of truth table for negative |
|  | RS & T flip flops. |  | edge triggered IC of JK flip-flops. |
|  |  |  |  |  |
|  | 2nd | Operation using waveforms and truth tables of D | 2nd | Verification of truth table for level |
|  | & Master/Slave flip flops. |  | triggered IC flip-flops of D latch |
|  |  |  |  |  |
|  |  | Operation using waveforms and truth tables of |  | Verification of truth table for level |
|  | 3rd | JK flip flops. | c) | 3rd | triggered IC of D flip-flop |
|  |  | Difference between a latch and | a flip flop |  |  |  |
|  |  |  |  |  |  |
| 11th |  | **9. Counters** |  |  | Verification of truth table for level |
|  | 1st | a) Introduction to Asynchronous and Synchronous | 1st | triggered IC of JK flip-flops. |
|  |  | counters |  |  |  |  |
|  | 2nd | b) Binary counters |  | 2nd | Verification of truth table for encoder |
|  |  |  | Ics |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  | 3rd | c) Divide by N ripple counters, Decade counter | 3rd | Verification of truth table for decoder |
|  |  |  | ICs |
|  |  |  |  |  |  |
| 12th | 1st | Ring counter |  | 1st | Verification of truth table for Mux |
|  |  | **10. Shift Register** |  |  | Verification of truth table for DeMux |
|  | 2nd | Introduction and basic concepts including shift | 2nd |  |
|  |  | left and shift right. |  |  |  |
|  |  |  |  |  |  |
|  |  | a) Serial in parallel out, serial in serial out |  |  | To design a 4 bit SISO shift registers |
|  | 3rd |  |  | 3rd | using JK/D flip flops and verification |
|  |  |  |  |  | of their operation. |
| 13th |  | Parallel in serial out, parallel in parallel out. |  |  | To design a 4 bit SIPO shift registers |
|  | 1st |  |  | 1st | using JK/D flip flops and verification |
|  |  |  |  |  | of their operation. |
|  |  |  |  |  |  |
|  |  | b) Universal shift register |  |  | To design a 4 bit PISO shift registers |
|  | 2nd |  |  | 2nd | using JK/D flip flops and verification |
|  |  |  |  |  | of their operation. |
|  |  |  |  |  |  |
|  |  | **11. A/D and D/A Converters** |  |  | To design a 4 bit PIPO shift registers |
|  | 3rd | Working principle of A/D and D/A converters | 3rd | using JK/D flip flops and verification |
|  |  |  |  |  | of their operation. |
| 14th |  | Brief idea about different techniques of A/D |  | To design a 4 bit ring counter and |
|  | 1st | conversion |  | 1st | verify its operation. |
|  | Study of | • Stair |  |
|  |  | step Ramp A/D converter |  |  |  |
|  |  |  |  |  |  |
|  | 2nd | • Dual Slope A/D converter |  | 2nd | To design a 4 bit ring counter and |
|  | • Successive Approximation A/D Converter | verify its operation. |
|  |  |  |  |  |  |
|  |  | Detail study of : |  |  | To design a 4 bit ring counter and |
|  | 3rd | • Binary Weighted D/A converter |  | 3rd | verify its operation. |
|  |  | • R/2R ladder D/A converter |  |  |  |
|  |  |  |  |  |  |
| 15th | 1st | • R/2R ladder D/A converter |  | 1st | Use of Asynchronous Counter ICs |
|  | Applications of A/D and D/A converter. |  | (7490 or 7493) |
|  |  |  |  |  |  |
|  |  | **12. Semiconductor Memories** |  |  | Use of Asynchronous Counter ICs |
|  | 2nd | Memory organization, classification of |  | 2nd | (7490 or 7493) |
|  | semiconductor memories (RAM, ROM, PROM, |  |
|  |  | EPROM, EEPROM) |  |  |  |
|  |  |  |  |  |
|  | 3rd | Static and dynamic RAM, Introduction to 74181 | 3rd | Use of Asynchronous Counter ICs |
|  | ALU IC |  | (7490 or 7493) |
|  |  |  |  |  |  |

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| --- | --- | --- | --- | --- |
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|  |  |  | ICs |
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